AMENDMENTS TO THE ABSTRACT

Please delete the section entitled "ABSTRACT OF THE DISCLOSURE" in its entirety and substitute the following section therefor:

ABSTRACT OF THE DISCLOSURE

A branch prediction apparatus that employs dual call/return stacks to predict return addresses in a microprocessor. The apparatus includes a first call/return stack that provides a speculative return address based upon a return instruction hit in a speculative branch target address cache (BTAC) of an instruction cache fetch address prior to decoding of the instruction to know whether it is actually a return instruction. The speculative return address is one of multiple return addresses simultaneously stored in the first call/return stack each pushed thereupon in response to the BTAC indicating a call instruction was fetched and prior to decoding the call instruction. The speculative return address is provided early in the pipeline and the microprocessor speculatively branches to the speculative return address. Later in the pipeline, a second call/return stack provides a non-speculative return address after the instruction is decoded and verified to be a return instruction. A comparator compares the speculative and non-speculative return addresses, and if the two addresses mismatch, the microprocessor branches to the non-speculative return address.